UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,900	09/22/2003	Kazi Asaduzzaman	174/277	2500

36981 7590 05/14/2007

FISH & NEAVE IP GROUP
ROPES & GRAY LLP
1211 AVENUE OF THE AMERICAS
NEW YORK, NY 10036-8704

EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2611	

MAIL DATE	DELIVERY MODE
05/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,900	ASADUZZAMAN ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,9-12,16-27 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,9-12,16-27 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 2/16/07 in which claims 2-6, 9-12 and 29-34. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-6, 9-12, 16- 27 and 32-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Huscroft et al U.S. Patent No 5,512,860.

As per claim 20 and 26, Huscroft et al teach an apparatus for receiving and processing a clock data recovery (CDR) signal comprising: reference clock signal processing circuitry (see fig.1) that receives as input a reference clock signal (see fig.1 element REFCLK) and is operative to produce a recovered clock (see fig.1 output of element 3 and col.4, lines 30-35) signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal (see fig.1 element 15); data recovery circuitry that receives as input the recovered clock signal and the CDR signal and is operative to phase align the recovered clock signal to the CDR signal, to use the recovered clock signal to recover clock information embedded in the CDR signal, and to use the clock information to recover data

information in the CDR signal (see fig.1 element 5 and col.4, line 26-65 and col.5, lines 1-10) ; a dynamically adjustable parts per million (PPM) detector operative to output a signal when a frequency difference between the reference clock signal and the recovered clock signal is within a predetermined frequency setting (see fig.1 element 23 and col.4, lines 65-67 and col.6, lines 8-20, 50-52 and col.7, lines 63-65 and col.8, lines 36-42); and control circuitry(see fig.1 element 19) that receives as input a first signal, a second signal (note that element 19 receives multiple inputs), and the output signal of the PPM detector (see output of element 23) and is operative to control the reference clock signal processing circuitry and the data recovery circuitry (see col.5, lines 55-67 and col.6, lines 15-20 and col.7, lines 18-30).

As per claim 2, Huscroft et al teach wherein the reference clock signal processing circuitry comprises a divider circuit (see fig.1 element 3 or 13) that divides the recovered clock signal by a predetermined scale factor.

As per claim 3, Huscroft et al teach wherein the reference clock signal processing circuitry further comprises: a phase frequency detector (see fig.1 element 15) that compares the phase and frequency of the reference clock signal and an output signal of the divider circuit, and outputs a signal indicative of whether the output signal of the divider circuit should be speeded up or slowed down to better match the phase and frequency of the reference clock signal (see fig.1 element 15).

As per claims 4 and 10, Huscroft et al teach wherein the reference clock signal processing circuitry further comprises: a charge pump (see col.7, lines 5-10) that receives as input the output signal of the phase frequency detector; and a loop filter that

receives as input the output of the charge pump to produce a voltage controlled oscillator current control signal (see fig.1 element 7 and col.7, lines 5-10).

As per claims 5 and 11, Huscroft et al teach wherein the reference clock signal further comprises: a voltage controlled oscillator that receives as input the voltage controlled oscillator current control signal and outputs the recovered clock signal that better matches the phase and frequency of the reference clock signal (see fig.1 element 1).

As per claim 6, Huscroft et al teach wherein the reference clock signal processing circuitry further comprises: a lock detector that receives as input the output signal of the phase frequency detector and outputs a signal indicative of whether a phase of the output signal of the divider circuit is similar to the phase of the reference clock signal (see fig.1 element 23).

As per claim 9, Huscroft et al teach wherein the data recovery circuitry further comprises a phase detector (see fig.1 element 5) that compares a phase of the recovered clock signal and the CDR signal and outputs a signal indicative of whether the recovered clock signal needs to be speeded up or slowed down to better match the phase of the CDR signal.

As per claims 12 and 22-25, Huscroft et al inherently teach wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry (note that element 19 receives multiple inputs): first, directs operation of the reference clock signal processing circuitry; and second, directs operation of the data recovery circuitry in response to receiving an output signal from

the reference clock signal processing circuitry indicating that the recovered clock signal has a phase and frequency similar to the phase and frequency of the reference clock signal (see col.5, lines 55-67 and col.6, lines 15-20 and col.7, lines 18-30).

As per claims 16 and 18, Huscroft et al inherently teach processing circuitry; a memory coupled to the processing circuitry (see col.9, line 50 and col.10, line 50).

As per claims 17 and 19, Huscroft et al inherently teach a VLSI (very large integrated circuit) which is the same or functionally equivalent to the claimed (printed circuit board) (see col.1, line 26) on which is mounted the apparatus as defined in claim [[i]] 20.

As per claims 21, Huscroft et al inherently teach wherein the predetermined frequency setting is dynamically adjustable and set by at least one of programmable logic resource core circuitry, circuitry external to programmable logic resource core circuitry, or user input.

As per claims 27 and 34, Huscroft et al inherently teach wherein processing the reference clock signal and the CDR signal comprises: processing in reference clock mode to produce [[a]] the recovered clock signal (see fig.1 element 15); and processing in data mode to phase align the recovered clock signal to the CDR signal, to use the recovered clock signal to recover clock information embedded in the CDR signal, and to use the clock information to recover the data information in the CDR signal (see fig.1 element 5).

As per claim 32, Huscroft et al inherently teach further comprising processing in reference clock mode when the first signal is set to a first logic value and the second signal is set to a second logic value.

As per claim 33, Huscroft et al inherently teach further comprising processing in data mode when the first signal is set to a first logic value and the second signal is set to a second logic value.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29-31 are rejected under 35 U.S.C. Dalmia U.S. Patent No 6,211.741 B1.

As per claims 29 and 31, Huscroft teaches all the features of the claimed invention except further comprising automatically switching from processing in reference clock mode to processing in data mode when the first signal is set to a first logic value, when the second signal is set to a second logic value, and when a frequency difference between the reference clock signal and the recovered clock signal is within a predetermined frequency setting.

Dalmia teaches a multiplexing for automatically switching (see figs.1-2 elements 22 and 152) from processing in reference clock mode (see element 14) to processing in data mode (see element 12) when the first signal is set to a first logic value, when the second signal is set to a second logic value, and when a frequency difference between

the reference clock signal and the recovered clock signal is within a predetermined frequency setting (see col.1, lines 42-47 and col.2, lines 65-67 and col.3, lines 45-50).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Dalmia into Huscroft as to lock the data signal and generate recovered data as taught by Dalmia (see col.1, lines 45-48).

As per claim 30, Huscroft and Dalmia in combination would teach wherein the predetermined frequency setting is dynamically adjustable as to accurately control the locking of the CDR circuit to the signal reference clock.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

5/4/2007

Emmanuel Bayard
Primary Examiner
Art Unit 2611

EMMANUEL BAYARD
PRIMARY EXAMINER